

Customer No.: 31561
Application No.: 10/064,882
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IN THE SPECIFICATION

Please amend the following text paragraph as follows.

[0019] Referring to Fig. 1 and Fig. 2, show a schematic top view of a hexagonal gate flash memory cell fabricated and a cross-sectional view of a hexagonal gate flash memory cell fabricated respectively, according to this invention. The radiation resistant hexagonal gate flash memory cell 100 includes a substrate 130, a source region 112 located within the substrate 130, a drain region 110 also located within the substrate 130 and a gate structure 120. The gate structure 120 is above the substrate 130 between the source region 112 and the drain region 110. The gate structure 120 further includes an oxide layer 120a, a nitride layer 120b, an oxide layer 120c and a control gate layer 120d. The oxide layer 120a, the nitride layer 120b and the oxide layer 120c together form an oxide-nitride-oxide (ONO) composite layer. The ONO layer and the control gate layer 120d are sequentially stacked over the substrate 130. As shown in Fig. 2, a channel region 140 is formed in the substrate 130 between the source region 112 and the drain region 110. A source region 112' as shown by the dotted line in Fig. 1 includes a portion of the gate structure 120 and the source region 112 that would be formed subsequent to programming the above gate flash memory cell.